UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/372,296	08/11/1999	ALTUG KOKER	42390.P6725	1235

7590 07/11/2003

BLAKELY SOKOLOFF
TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025

EXAMINER	
SONG, JASMINE	

ART UNIT	PAPER NUMBER
2188	18

DATE MAILED: 07/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 18

Application Number: 09/372,296
Filing Date: August 11, 1999
Appellant(s): KOKER ET AL.

Thinh V. Nguyen
Reg. No. 42,034
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 04/28/2003.

(1) Real Party of Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal is contained in the brief.

(3) Status of the Claims

The statement of the status of the claims contained in the brief is correct. The appeal involves claims 1-21.

(4) Status of Amendments

The appellant's statement of the status of amendments after final rejection contained in the brief is incorrect.

The response filed December 23,2002 was referred to by the appellants as an amendment. However, in that response, the appellants did not request any amendments to the application. Accordingly, the response filed December 23, 2002 was treated as a request for reconsideration.

(5) Summary of the Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of the Claims

Claims 1-21 stand or fall together because the appellant's brief contains the statement that "the claims of the present invention stand or fall together".

(8) Claims under Appeal

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of the claims under appeal.

6,216,208	GREINER et al.	4-2001
6,356,962 B1	KASPER	3-2002

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1,4-5,8 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Greiner et al., U.S. Patent 6,216,208.

Regarding claims 1, 8 and 15, Greiner et al. teach a system comprising:

a memory is taught as external memory (col.2, lines 15-16 and lines 56);

a bus is taught as the memory bus or CPU bus(Fig. 1, element 300); and

a bus access circuit (Fig.1, element 100) coupled to the memory and the bus (Fig.1) to reduce latency in accessing the memory from the bus, the circuit comprising:

a pre-fetcher (Fig.1, prefetch queue) to pre-fetch a plurality of data from the memory (external memory) to a data queue (Fig.1, element 120) in response to a request (col.2, lines 59 to col.3, lines 10), and

a queue controller is taught as a cache controller coupled to the data queue (Fig.1, element 120) and the pre-fetcher to deliver the pre-fetched data (the prefetched data stored in the 120) from the data queue to the bus (CPU bus) independently of the memory (external memory)(col.5, lines 46-58).

Regarding claim 4, Greiner et al. teach that determining if the request is valid and processing a cache miss request if the request results in a cache miss is taught as the internal queue monitors the requests issued by the arbiter, and monitors data held by the cache to determine whether a copy of the requested location is held in the cache (col.2, lines 54-62).

Regarding claim 5, Greiner et al. teach that the processing of the cache miss request comprises: Providing a purge signal, marking an entry in a scheduler according to the purge signal; purging data corresponding to the marked entry (Fig.3,step 1030-

1070-1090 and col.5, lines 7-17); and placing the request to the memory controller (col.5, lines 37-49).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3,9-12 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greiner et al., U.S. Patent 6216208, in view of Kasper, U.S. Patent 6,356,962.

Regarding claim 2, 9 and 16, Greiner et al. teach the claimed invention (claims 1,8 and 15) and the request causes the memory controller transferring the plurality of data to the data queue (col.2, lines 59 to col.3, lines 32), the request being buffered in a request queue (Fig.1, element 130 and col.2, lines 37-38).

Greiner does not teach that a watermark monitor is used to determine if an amount of data in the data queue is above a predetermined level, if not, the request causing the memory controller to transfer the plurality of data to the data queue.

However, Kasper teaches that a watermark is used to determine if an amount of data in the data queue is above a predetermined level, if not, the request causing the memory controller to transfer the plurality of data to the data queue (col.4, lines 7-14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ a watermark monitor to indicate that sufficient storage exists in the FIFO memory to receive additional data as taught by Kasper in the Greiner's system because it effectively increases bus and memory resource utilization (col.3, lines 35-42 and col.1, lines 9-11).

Therefore, one having ordinary skill in the art at the time the invention was made would have been motivated to provide a watermark monitor in the Greiner's system because it would provide a "window" into the FIFO memory (col.3, lines 52-53) allowing the controller to transfer the data to the FIFO memory.

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claims 3,10 and 17, Greiner et al. teach transferring the data from the data queue to the bus if the data in the data queue are ready. It is obvious that the data are transferred when the data are ready because the data must be ready before they are transferred (col.5, lines 46-58).

Regarding claims 11 and 18, Greiner et al. teach a peripheral bus controller (Fig.1, element 110) coupled to the bus (Fig.1, the line connected 110 and 130) and the pre-fetcher (Fig.1, element 160) to determine if the request is valid (col.2, lines 54-62);

a data coherence controller (Fig.2, element 170) coupled to the pre-fetcher to provide a purge signal (a buffer entry pointed by a pointer, col.5, lines 7-17) when the request corresponds to a cache miss (col.5, lines 7-17 and col.2, lines 54-62); and

a scheduler (Fig.2, element 110) coupled to the request queue (Fig.1, element 130) and the data coherence controller (Fig.2, element 170) to store entries corresponding to the requests, the entries being marked according to the purge signal from the data coherence controller (Fig.3,step 1030-1070-1090 and col.5, lines 7-17).

Regarding claims 12 and 19, Greiner et al. teach processing the cache miss request comprises:

a data mover (Fig.1, element 140) coupled to the data queue and the scheduler to transfer data from the memory to the data queue (col.2, lines 59 to col.3, lines 32), the data mover purging data corresponding to a marked entry from the scheduler (Fig.3,step 1030-1070-1090 and col.5, lines 7-17);

Claim 6-7,13-14 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greiner et al., U.S. Patent 6,216,208 B1.

Regarding claims 6,13 and 20, Greiner teaches the claimed independent claims as noted above. Greiner does not teach that the bus is a peripheral component interconnect bus (PCI bus). Official notice is taken that it is well know in the art that PCI bus is one of the most widely used types of buses. It would have been obvious to one of

ordinary skill in the art at the time the invention was made to use PCI bus in Greiner's bus system because PCI bus is an industry standard bus.

Regarding claims 7,14 and 21, Greiner teaches the claimed independent claims as noted above. Greiner does not teach that the request is one of a 32-byte and a 64-byte requests. It is well know in the art that 32-byte or 64-byte data request is commonly used. It is also an obvious matter of design choice to use one of a 32-byte and 64-byte requests in Greiner's requested data, since these are power of 2.

(11) Response to Argument

In response to appellant's argument that "the prefetch queue receives the address information from the internal queue, not from a memory" on page 7, third paragraph of the Brief, in the office Action of paper No.12, the Examiner indicated that the data queue is element 120 in the Fig.1 of the Greiner and the data in the element 120 is prefetched from the external memory (col.2, lines 54-58 and col.3, lines 7-10 and col.5, lines 55-56).

In response to appellant's argument that "the element 162 is an address buffer to store addresses associated with the request, not the data" on page 7, third paragraph of the Brief, after carefully reviewing the Greiner reference, the Examiner agrees that the element 162 is an address buffer which stories addresses associated with previous read requests. The address buffer 162 is used by Greiner to determine when the processor core is executing sequential addresses and therefore might benefit from prefetching.

However, the Examiner notes that the appellant's argument is not related to the limitations claimed in the claims 1,8 and 15.

In response to appellant's argument that "the data are delivered to the core, not to a bus independently of the memory" on page 7, last line to page 8, first line of the Brief, the Examiner notes that the prefetched data from the external memory are stored in the cache 120 and then delivered to the core 200 using the CPU bus (the bus connected between the cache 120 and core 200 as shown in Fig.1) without resorting to the slower external bus 300 which connects the external memory (col. 5, lines 55-58). Therefore, the prefetched data are delivered to the core independently of the external memory.

In response to appellant's argument that "Greiner does not disclose prefetching data from a memory to a data queue **in response to a request**" (emphasis added), the examiner noted that this limitation is taught in col.2, lines 54-58 and col.3, lines 7-10 and col.5, lines 55-56.

In response to appellant's argument that " the very fact the PCI bus was well known in the art at the time of Greiner but was not taught by Greiner indicates that it was not obvious to modify Greiner" on page 9 of Brief, the Examiner notes that the absence of an element from a reference does not logically mean that it would not be obvious to add that element to the reference. If this were true, then it would never be

obvious to add an element to a reference. Furthermore, it is noted that in appellant's responses dated July 30, 202 and January 2, 2003 failed to officially traverse the Examiner's assertion official notice. Therefore, the Examiner's assertion of official notice is taken to be admitted prior art (See MPEP 2144.03 (c)).

In response to appellant's argument that there is no suggestion to combine the references in the fourth and sixth paragraphs on page 9 of Brief, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ a watermark monitor to indicate that sufficient storage exists in the FIFO memory to receive additional data as taught by Kasper in the Greiner's system because it effectively increases bus and memory resource utilization as stated above (col.3, lines 35-42 and col.1, lines 9-11 in Kasper's reference).

The Examiner cited that "a bus is taught as the memory bus or CPU bus (Fig.1, element 300)" in the rejection of claim 15. The examiner did not exactly cite a label for the CPU bus, but the CPU bus is the bus connected between the cache 120 and core

200 passing through the arbiter 110 as shown in Fig.1. In order to make it clear regarding the bus, the Examiner has two interpretations: if the bus is the CPU bus, then the prefetched data from external memory stored in the cache 120 will be delivered to the processor core on the CPU bus independently of the external memory; if the bus is the external bus 300, then the prefetched data from external memory stored in the cache 120 will be delivered to another processor or devices on the external bus independently of the external memory. Therefore, "a bus" in claim 15 can be either the CPU bus or the external bus, and the limitation will be met.

In summary, the prefetched data stored in the cache 120 would be delivered to processor core 200 (or other processor/devices on the external bus 300) independently of external memory since the data is already prefetched from the external memory. Therefore, the limitation in claims 1,8 and 15 are met.

Respectfully Submitted,

Jasmine Song
Patent Examiner
Art Unit 2188

Kevin Verbrugge
Primary Examiner
Art Unit 2188
Conferee

Donald Sparks
Supervisory Patent Examiner
Art Unit 2187
Conferee

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 Wilshire Blvd., 7th Floor
Los Angeles, California 90025